REMARKS

Claims 1-20 remain present in this Office Action, all of which have been rejected. In the present Office Action, claims 1-20 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite; claims 1-5, 7, 10-15, 17 and 18 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,536,717 (hereinafter Hauge); and claims 6 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hauge. At the outset, Applicant submits that original claims 1, 3, 10, 13 and 17 are definite in the context of the specification. However, Applicant has nevertheless amended the claims for clarification and to address the §112 rejections, as doing so does not narrow the scope of the claims. Applicant has also amended claims 19 and 20 for clarification of Applicant's claimed subject matter. For the reasons that are further set forth below, Applicant respectfully submits that all of claims 1-20 are now allowable over the applied prior art of record.

Applicant believes that a brief review of Applicant's claimed subject matter may help move this case toward allowance. As is disclosed in Applicant's specification, paragraph 6, due to the nature of bipolar transistors and their need for a finite amount of base drive current for operation, design of circuitry that compares a voltage on a timing capacitor to a predefined reference voltage becomes problematic given the need to limit perturbations to the charging current of the timing capacitor. Additionally, blinding timer circuitry, which may be tied to the timing capacitor, represents another possible source of error current. As is disclosed in Applicant's specification, paragraph 18, according to various embodiments of the present invention, a technique for reducing input currents associated with a comparator circuit during certain events is disclosed. According to the technique, bias currents associated with the comparator circuit are minimized when a difference between a magnitude of an input signal (at a signal input of the comparator circuit) and a magnitude of a reference signal (applied to a reference input of the comparator circuit) is greater than a predetermined value. The

bias currents associated with the comparator circuit are then increased when the difference between the magnitudes of the input signal and the reference signal are substantially similar, e.g., within 50mV of each other. With reference to Applicant's specification, paragraph 21, this normally provides a substantial reduction in input currents while preserving the accuracy of the comparator function.

Additionally, according to the present invention, a blinding timer function may be included that is designed to limit the amount of leakage current attributable to a discharge current source that is coupled to the timing capacitor. As is disclosed in Applicant's specification, paragraph 23, any voltage difference becomes an offset error voltage in the comparator 20. Providing matched bias currents for outer transistors 21 and 22 serve to increase the gain of the transistors 21 and 22, which overcomes base current differences in the inner transistors 23 and 24 and creates equal base-to-emitter voltages (Vbes) in the outer two transistors 21 and 22, which increases the accuracy of the comparator 20. However, as is set forth in Applicant's specification, paragraph 24, matching accuracy for a comparator is only important at the point that the voltages being compared are substantially equal. Thus, when the voltages being compared are substantially different, the comparator is fully switched to a given state and there is no need to be concerned with mismatch-based errors in the circuit. Accordingly, the bias currents for the outer transistors can be essentially eliminated during the periods of large input differences. This also substantially reduces timing errors associated with comparator input currents. Thus, as set forth in independent claims 1, 10 and 17, as amended, when a difference between a magnitude of an input signal and a magnitude of a reference signal is greater than a predetermined value, the bias currents are minimized. However, the bias control circuitry increases the bias currents associated with the comparator circuit when the difference between the magnitude of the input signal and the magnitude of the reference signal is less than the predetermined value.

With reference again to the Office Action, the Examiner has based various 35 U.S.C. §112, second paragraph, rejections on a number of criteria. For example, the Office Action states that "Figure 3 of the present application shows that the 'bias currents **associated** with the first and second transistors (Q1, Q2) is bias current source (I1). The bias current (I1) is fixed because (I1) is a constant current source. It is not clear what 'bias current **associated** with the first and second transistors' is meant by. As understood by the examiner, the recited 'bias current' is the current flowing through transistor (Q1) or (Q4). This is merely the collector-emitter current, not the bias current. The Applicant is requested to clarify what are the 'bias currents associated with the first and second transistors.'"

Initially, Applicant notes that the term "bias currents" is a well-established term in the art and refers the Examiner to Hauge, column 5, lines 3-4, which references Hauge Fig. 3, and states "[t]ransistors 90, 92 act as current sources to provide bias current for transistors 58 and 64." Further, as is stated in Applicant's specification, paragraph 28, and with reference to Fig. 3, various current mirrors are depicted as current sources to simplify the explanation of operation. When the differential input voltages are such that Vin is much less than Vref, i.e., the condition corresponding to early stages of capacitor C1 charging, transistors Q1 and Q2 are in an off-state with transistor Q3 conducting all the current pulled by current source I3. A diode connected PNP transistor Q6 serves to form the reference for the current mirror composed of transistors Q5, Q6, Q7 and Q8. With the transistor Q6 also conducting a bias current equal to 2Ibias, the transistor Q8 conducts approximately the same current. The transistor Q7 conducts a current less than that conducted by the transistors Q6 and Q8, due to the presence of resistor R10 connected to the emitter of the transistor Q7. With regard to the timer comparator output state, the transistor Q8 collector current of approximately 2Ibias exceeds the current pulled by current source I4, thereby turning on transistor Q9 and pulling output COMPOUT low.

With reference to Applicant's specification, paragraph 29, the transistor Q7 collector current, which is slightly less than 2Ibias, exceeds the current pulled by current source I1, reverse biasing diodes D1 and D2. With the diodes D1 and D2 reverse biased, there is no bias current applied to the transistors Q1 and Q4. With reference to Applicant's specification, paragraph 30, as the voltage on the capacitor C1 approaches Vref, the current supplied by the current source I3 becomes split between the transistors Q2 and Q3. At Vin equal to Vref, the current is equally split between the transistors Q2 and Q3. With the transistors Q2 and Q3 equally splitting the current sourced by the current source I3, the current through the transistor Q6 is Ibias. Again, the transistor Q7 conducts less than Ibias due to the presence of the resistor R10. With less than Ibias sourced onto the common node between the diodes D1 and D2, the current source I1 forward biases the diodes D1 and D2 with equal currents. These diode currents become bias currents for the transistors Q1 and Q4, creating the matched bias conditions desired for best accuracy. With reference to Applicant's specification, paragraph 31, the actual balance point bias of the transistors Q1 and Q4 is determined by the choice of value of the resistor R10, which reduces the current in the transistor Q7 relative to that in the other transistors in the PNP current mirror rail.

With reference to the 35 U.S.C. §112, second paragraph, rejections of claims 8 and 19, the Office Action states that "'a blinding timer discharge current source...' is indefinite because it is not clear what it is and how it is connected to capacitor C1 in figures 3 or 6." Applicant directs the Examiner to Applicant's specification, paragraph 33, which fully describes a blinding timer circuitry discharge source 50. With reference to Applicant's specification, paragraph 37, the components of the blinding timer capacitor discharge current source in Fig. 6 are further described. The Office Action further states that "claim 20...is indefinite because it is not clear. Figure 6 of the present application shows that switch (Q24) coupled to capacitor (C1) itself cannot reduce its own leakage current." Applicant refers the Examiner to Applicant's

specification, paragraph 34, which describes a circuit, which includes a transistor Q24 and a diode coupled transistor Q108 (as well as a resistor 76) that acts as a switch.

Turning again to the rejection of independent claims 1, 10 and 17, as being anticipated by Hauge, Applicant respectfully submits that Hauge does not teach a comparator circuit that controls bias currents associated with the outer transistors of the comparator circuit dependent upon an input signal proximity to a reference voltage. More specifically, Hauge merely discloses a comparator circuit that functions, as is disclosed in Applicant's background, i.e., a comparator circuit that always provides bias currents to the outer transistors. Thus, Hauge does not teach, nor does Hauge suggest, bias current control circuitry for controlling bias currents associated with first and second transistors associated with an outer transistor stage of a comparator circuit that minimizes bias current when a difference between a magnitude of an input signal (at a signal input terminal) and a magnitude of a reference signal (applied to a reference input terminal) is greater than a predetermined value. Nor does Hauge teach or suggest bias current control circuitry that increases bias currents associated with a comparator circuit when the difference between the magnitude of the input signal (at the signal input terminal) and the magnitude of the reference signal (at the reference input terminal) is less than the predetermined value. Column 4 of Hauge merely states that proper biasing of the output transistors 18 and 24 is provided by DC current source 26. For at least these reasons, Applicant submits that independent claims 1, 10 and 17 are allowable over Hauge. Further, Applicant submits that claims 2-9, 11-16 and 18-20 are also allowable for at least the reason that they depend upon an allowable claim.

Applicant respectfully submits that this reply is fully responsive to the above-referenced Office Action.

CONCLUSION

For at least all of the foregoing reasons, Applicant respectfully submits that claims 1-20, as amended, are now allowable. If the Examiner has any questions or comments with respect to this reply, the Examiner is invited to contact the undersigned at (616) 949-9610.

Respectfully submitted,

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By: PRICE, HENEVELD, COOPER, DEWITT & LITTON, LLP

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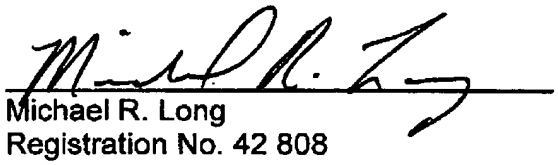

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